Q.P. Code: **16EC5703** **R16**

Reg. No: | | | | | | | | | | |

SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLOGY:: PUTTUR
(AUTONOMOUS)
M.Tech I Year I Semester (R16) Regular Examinations January 2017
DIGITAL IC DESIGN
(VLSI)
(For Students admitted in 2016 only)

Time: **3 hours** Max. Marks: **60**

(Answer all Five Units **5 X 12 =60** Marks)

UNIT-I

Q.1	a	Give the advantages of dynamic logic over static CMOS logic?	7M
	b	With a neat sketch explain the circuit topology and operation of CMOS domino logic	5M

OR

Q.2	a	How does the domino logic solves the dynamic logic problem?	4M
	b	How is dynamic CMOS circuits faster than static CMOS circuits?	8M

UNIT-II

Q.3	a	Draw the schematic diagram of a SRAM memory cell along with sense amplifier and data write circuitry and explain.	6M
	b	Explain the logical effort of two – input NAND and NOR gates with neat circuit diagram	6M

OR

Q.4	a	What are the design considerations of a 4 bit RAM with the help of CMOS logic diagram.	5M
	b	Draw one cell dynamic RAM circuit and explain its working.	7M

UNIT-III

Q.5	a	Elaborate on delay and power consumption in BICMOS logic circuits.	6M
	b	What are the advantages and disadvantages of BiCMOS	6M

OR

Q.6	a	Explain in detail about bipolar gate design with neat sketches.	7M
	b	Give the schematic diagram of different Bi-CMOS inverters. Explain its operation	5M

UNIT-IV

Q.7	a	Explain: (i) Area capacitance.	6M
	b	What is the need of wired capacitance? Where it is used? Explain.	6M

OR

Q.8	a	Explain two input NAND gate with relevant Layout example.	7M
	b	How do you determine the capacitance of a MOS capacitor	5M

UNIT-V

Q.9	a	Analyze the timing of the array multiplier and explain.	7M
	b	With a neat sketch explain the working of array multiplier	5M

OR

Q.10	a	What are the design approach of 4 bit shifter	5M
	b	Draw and explain the booth decode cell used for booth multiplier	7M

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